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12EC121

M.Tech. Degree Examination, Dec.2013/Jan.2014
Digital System Design Using Verilog

Time: 3 hrs. Max. Marks:100

Note: *1. Answer any FIVE full questions.*
2. Assume suitable data wherever required.
3. Mention top level blocks with input-output ports.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

1 a. Design the logic circuit shown in Fig.Q.1(a) for a night light that is lit only when the switch is ON and the light sensor shows that it is dark. The logic is to be realized using 2:1 MUX only. If there are three lamps in the room controlled using the same logic, how do you modify the circuit shown in Fig.Q.1(a). **(10 Marks)**

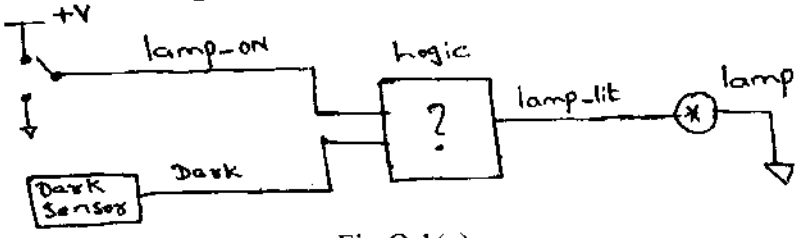

Fig.Q.1(a)

b. With the help of a detailed flow chart, discuss VLSI design flow. Mention the importance of each step in design flow. **(10 Marks)**

2 a. Ink jet printer have six catridge's for different colored ink: Black, Cyan, Magenta, Yellow, Light Cyan and Light Magenta. A multibit signal in such a printer indicates selection of one of the colors. To print the colors stored in different drums drivers need to be enabled for each of the colors.

i) Devise a minimal length code for the signal selection representing each color.
ii) Design the logic shown in Fig.Q.2(a) that can enable the corresponding driver based on the multibit signal.
iii) If the number of colors are increased from 6 to 8, discuss the necessary changes to be made to the multibit signal and the logic. **(10 Marks)**

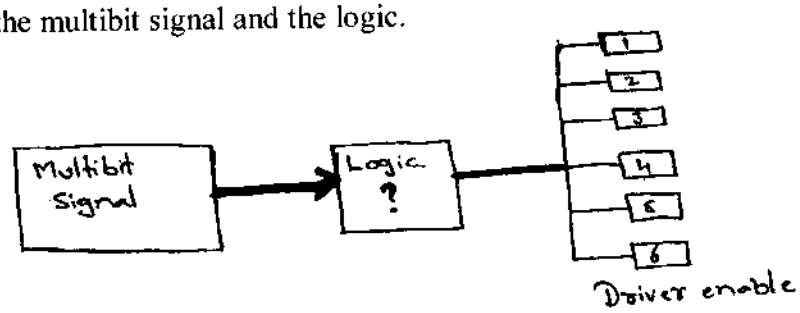

Fig.Q.2(a)

b. Write a verilog code for 10:1 multiplexer using case statement. **(10 Marks)**

3 a. Design a 4-bit unsigned combinational multiplier using 4-bit adder. **(10 Marks)**
b. Discuss fixed point and floating point number format with example. **(10 Marks)**

4 a. Write verilog code for a positive edge triggered flip-flop with clock enable, positive logic asynchronous preset and clear and both active high and active low outputs. It is illegal for both preset and clear to be active together. **(10 Marks)**

b. Develop a datapath to perform complex multiplication of two complex numbers a and b represented as a = ar + jai and b = br + jbi. The data path need to perform sequential complex multiplication, with shared resources and register to store intermediate results. Mention the control signals for the sequential datapath and discuss its working principle. **(10 Marks)**

5 a. Design a 64K × 16bit composite memory using 16K × 8 bit memory component. **(10 Marks)**

b. Develop a verilog code for a 32 × 7 bit Rom, that can store the data shown in Table Q.5(b).

Table Q.5(b)

Address	Content	Address	Content
0	0000001	6	1111111
1	0000011	7	1111110
2	0000111	8	1111100
3	0001111	9	1111000
4	0011111	10-15	0000000
5	0111111	16-31	1010101

(10 Marks)

6 a. Discuss the internal architecture of FPGA, highlighting the functionality of each modules. **(10 Marks)**

b. Define signal integrity, discuss ground bounce issue in signal integrity and mention the technique adopted to reduce ground bounce effect. **(10 Marks)**

7 a. With a neat block diagram discuss the organization of a high performance embedded computer with multiple buses. **(08 Marks)**

b. Write instructions that increment a 16-bit unsigned integer stored in memory. The address of the least significant byte is in r2. The most significant byte is in the next memory location. **(06 Marks)**

c. Discuss the importance of cache memory. how is cache memory used in a embedded processor. **(06 Marks)**

8 a. Discuss physical design flow and mention the importance of floor planning in physical design. **(06 Marks)**

b. Briefly discuss serial interface standards for I/O devices. **(06 Marks)**

c. Develop verilog code for 4-bit counter. **(08 Marks)**

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